WE CLAIM:

1. A method of forming an electronic component having elevated active areas, the method comprising:

providing a semiconductor substrate in a processing chamber, the semiconductor substrate having disposed thereon a gate electrode and exposed active areas;

performing a deposition process in which a silicon-source gas is supplied into the processing chamber to cause a polycrystalline layer to be deposited on the gate electrode and an epitaxial layer to be deposited on the active areas; and

performing a flash etch back process in which the polycrystalline layer is etched from the gate at a first etching rate and the epitaxial layer is etched from the active areas at a second etching rate, wherein the first etching rate is faster than the second etching rate.

2. The method of Claim 1, wherein the semiconductor substrate further comprises a dielectric region, and wherein deposition on the dielectric region is substantially avoided during the deposition process.

3. The method of Claim 1, wherein an etchant is also supplied into the processing chamber during the deposition process.

4. The method of Claim 3, wherein the etchant is hydrochloric acid.

5. The method of Claim 1, further comprising repeating the deposition process and the flash etch back process a plurality of times.

6. The method of Claim 1, wherein the gate is elevated with respect to the active areas, such that during the flash etch back process the polycrystalline layer is etched in two orthogonal dimensions.

7. The method of Claim 6, wherein after the flash etch back process is performed, no polycrystalline layer extends over a region directly above the active areas.

8. The method of Claim 7, wherein no polycrystalline material is left on the gate electrode after repeating the deposition process and the flash etch back process a plurality of times.

9. The method of Claim 1, wherein the deposition of the polycrystalline layer and the deposition of the epitaxial layer occur simultaneously.

10. The method of Claim 1, wherein no deposition takes place during the flash etch back process.

11. The method of Claim 1, wherein the deposition process is conducted at a lower temperature than the flash etch back process.

12. The method of Claim 11, wherein the processing chamber is heated to a temperature between approximately 400°C and approximately 1200°C before the flash etch back process is commenced.

13. The method of Claim 1, wherein the processing chamber is heated to a temperature between approximately 400°C and approximately 1200°C before the flash etch back process is commenced.

14. The method of Claim 1, wherein hydrochloric acid is supplied to the processing chamber during the flash etch back process.

15. The method of Claim 1, wherein the processing chamber is held at a pressure substantially equal to atmospheric pressure during the flash etch back process.

16. A method comprising:

providing a semiconductor substrate having a gate and exposed active areas;

depositing polycrystalline silicon on the gate and epitaxial silicon on the active areas in a first process step;

etching polycrystalline silicon from the gate in a second process step; and

repeating the first and second process steps a plurality of times.

17. The method of Claim 16, wherein the semiconductor substrate further comprises an oxide region, and wherein no silicon is deposited on the oxide region during the first process step.

18. The method of Claim 16, wherein during the second process step polycrystalline silicon is etched in two orthogonal dimensions.

19. The method of Claim 18, wherein after the first and second process steps are repeated a plurality of times, substantially no polycrystalline silicon exists in a region directly above the active areas.

20. The method of Claim 19, wherein substantially no polycrystalline silicon exists on the gate after repeating the first and second process steps a plurality of times.

21. The method of Claim 16, wherein during the first process step, polycrystalline silicon deposition and epitaxial silicon deposition occur simultaneously.

22. The method of Claim 16, wherein the second process step comprises simultaneously etching epitaxial silicon from the active areas.

23. The method of Claim 22, wherein the polycrystalline silicon is etched from the gate faster than the epitaxial silicon is etched from the active areas during the second process step.

24. The method of Claim 16, wherein silicon is not deposited onto the semiconductor substrate during the second process step.

25. The method of Claim 16, wherein the first process step is conducted at a lower temperature than the second process step.

26. The method of Claim 25, wherein the second process step is conducted a temperature between approximately 800°C and approximately 1200°C.

27. The method of Claim 16, wherein the second process step is conducted a temperature of approximately 800°C and approximately 1200°C.

28. The method of Claim 16, wherein the semiconductor substrate is exposed to hydrochloric acid during the second process step.

29. The method of Claim 16, wherein the semiconductor substrate is held at a pressure substantially equal to atmospheric pressure during the second process step.

30. A method comprising:

providing a semiconductor substrate in a processing chamber, the semiconductor substrate having a first surface and a second surface;

simultaneously performing epitaxial growth at an epitaxial growth rate over a first growth surface and polycrystalline growth at a polycrystalline growth rate over a second growth surface; and

controlling the epitaxial growth rate and the polycrystalline growth rate by periodically pausing the epitaxial growth and the polycrystalline growth to perform a flash etch back process, such that after the flash etch back process there is more

epitaxial growth on the first growth surface than polycrystalline growth on the second growth surface.

31. The method of Claim 30, wherein the semiconductor substrate further comprises an insulating region over which substantially no deposition occurs during the epitaxial growth and the polycrystalline growth.

32. The method of Claim 31, wherein an etchant is supplied into the processing chamber during the epitaxial growth and the polycrystalline growth.

33. The method of Claim 32, wherein the etchant is hydrochloric acid.

34. The method of Claim 30, wherein the epitaxial growth and the polycrystalline growth are conducted at a lower temperature than the flash etch back process.

35. The method of Claim 30, wherein hydrochloric acid is supplied to the processing chamber during the flash etch back process.

36. A method comprising:

providing a semiconductor substrate in a processing chamber having at least one oxide region and at least one non-oxide region; and

alternating a selective epitaxial growth process, during which epitaxial growth comprising polycrystalline growth and monocrystalline growth occurs in the at least one non-oxide region and during which substantially no deposition occurs in the at least one oxide region, with a flash etch back process, during which at least a portion of the polycrystalline growth is etched from the at least one non-oxide region.

37. The method of Claim 36, wherein an etchant is supplied into the processing chamber during the selective epitaxial growth process.

38. The method of Claim 37, wherein the etchant is hydrochloric acid.

39. The method of Claim 36, wherein during the flash etch back process the polycrystalline growth is etched in two orthogonal dimensions.

40. The method of Claim 36, wherein the deposition process is conducted at a lower temperature than the flash etch back process.

41. The method of Claim 36, wherein hydrochloric acid is supplied to the processing chamber during the flash etch back process.